CLAIMS

I CLAIM:

1. A method of measuring a data signal to create an eye diagram of that signal, the method comprising the steps of:

(a) setting a hits count to zero;

(b) comparing the instantaneous voltage of a clock signal associated with the data signal to a clock threshold voltage to produce a logical clock signal;

(c) delaying the logical clock signal by a selected first amount to produce a delayed logical clock signal;

(d) comparing the instantaneous voltage of the data signal to be measured to a data threshold voltage to produce a logical data signal;

(e) delaying the logical data signal by a selected second amount to produce a delayed logical data signal;

(f) delaying the delayed logical clock signal by a selected third amount to produce a doubly delayed logical clock signal;

(g) capturing the value of the delayed logical data signal in response to the delayed logical clock signal;

(h) capturing the value of the delayed logical data signal in response to the doubly delayed logical clock signal;

(i) incrementing the hits count each time a value captured in step (g) is different to that captured in step (h);

(j) repeating steps (b) through (i) until a selected condition is satisfied;

(k) subsequent to step (j), storing the count of step (i) in a data structure indexed by the difference between the first and second amounts and by the data threshold voltage;

(l) repeating steps (a) through (k) with different combinations of the data threshold voltage and difference between the first and second amounts; and

(m) generating an eye diagram from the hits counts stored in the data structure.

2. An eye diagram analyzer comprising:

a variable clock signal waveform delay circuit having an input for receiving a clock signal and an output producing a delayed clock signal;

a threshold detector having a variable threshold, an input for receiving a data signal to be measured as an eye diagram and having an output producing a logical data signal;

a variable data signal waveform delay circuit having an input coupled to receive the logical data signal and an output producing a delayed logical data signal;

a transition detection circuit coupled to the delayed clock signal and to the delayed logical data signal, and having an output producing a transition signal indicative of a transition in the delayed logical data signal occurring during a selected length of time subsequent to a transition in the delayed clock signal;

a counter coupled to the transition signal and that counts occurrences thereof; and

a memory whose content is organized as a data structure indexed by the difference in delays for the variable clock signal waveform delay circuit and the variable data signal waveform delay circuit, by the variable threshold, and that stores in an indexed location the number of counted occurrences.